



SIST 2011

FPGA beam loss monitor system for the SRF facility

By

Diana P. Perea

Benedict College



Supervisor: Jin-Yuan Wu

Fermi National Accelerator Laboratory

August 9, 2011.

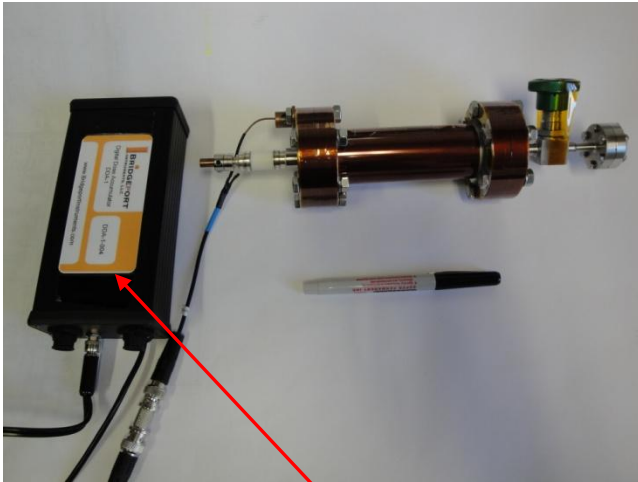
Outline

- ✓ What is a beam loss monitor(BLM) system?
- ✓ Describe Helium Ionization beam loss monitor
- ✓ Recycling Integrator for the signal processing
- ✓ Field Programmable Gate Array (FPGA)-based Time-to-Digital Converter (TDC)
- ✓ Show a brief display of the entire BLM system
- ✓ Test of the FPGA-TDC

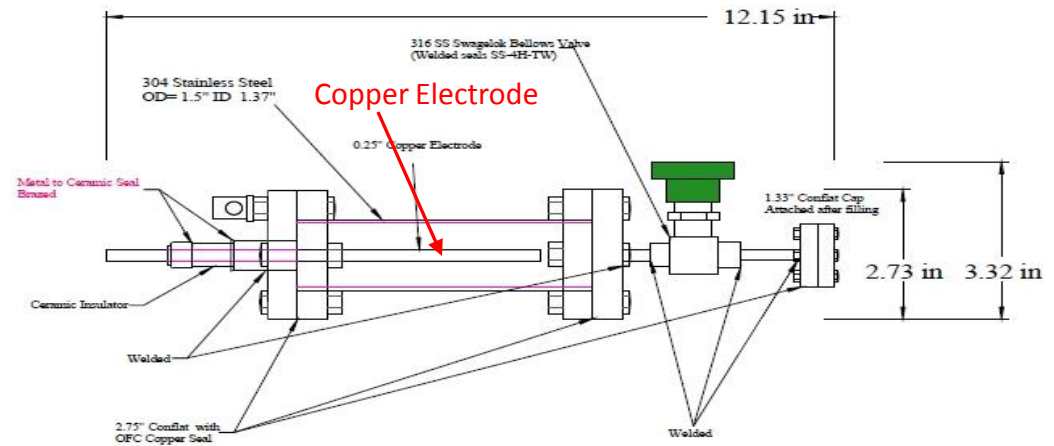
Beam loss monitor system

- The BLM systems are designed for measuring beam losses around an accelerator or storage ring.
- These systems give a useful beam diagnostics and machine protection from radiation damage.

He-Ionization Chamber Beam loss monitor



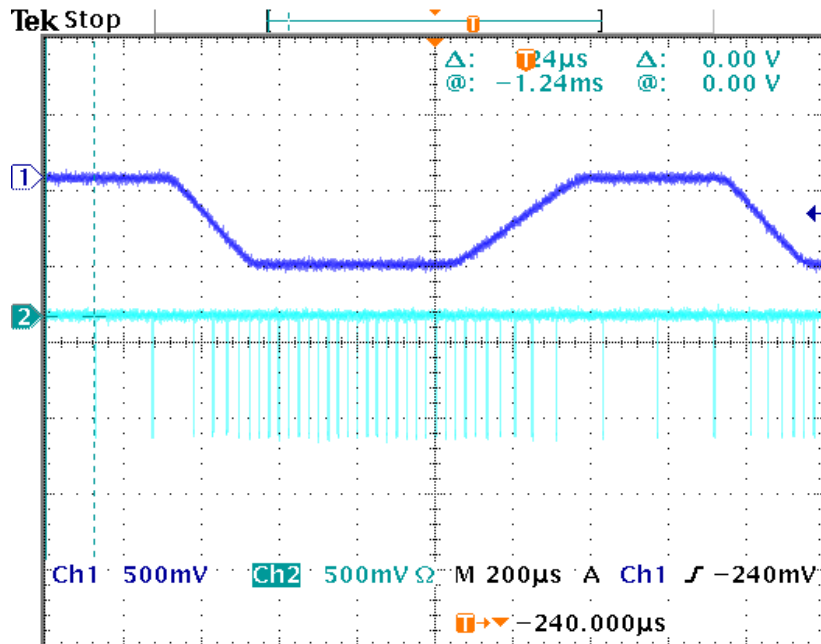
Electronics(Recycling Integrator)



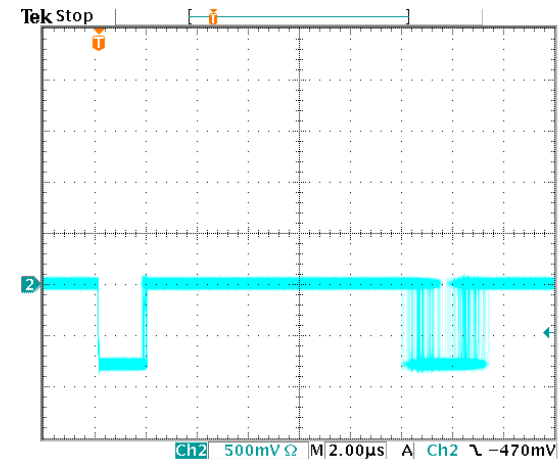
- ❖ Operation in air and high vacuum
- ❖ Operates from 5K to 350K
- ❖ Stainless steel vessel, 120cm³, filled with He-gas
- ❖ He-gas filling at 1.0- 1.5 bar pressure
- ❖ Sensitivity: 1.9 pA/(Rad/hr)
- ❖ Readout via current-to-frequency converter (1.9 Hz/(Rad/hr)) and FPGA-TDC
- ❖ Pulses can be sent through long cables

Recycling Integrator

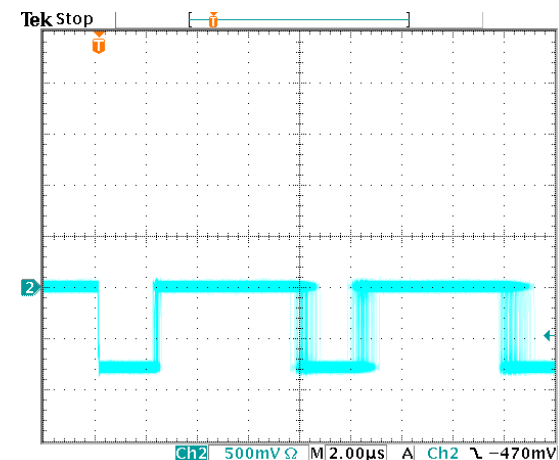
It generates pulses from current signals



Ch 1 represents input current, Ch2 output pulses from the recycling integrator



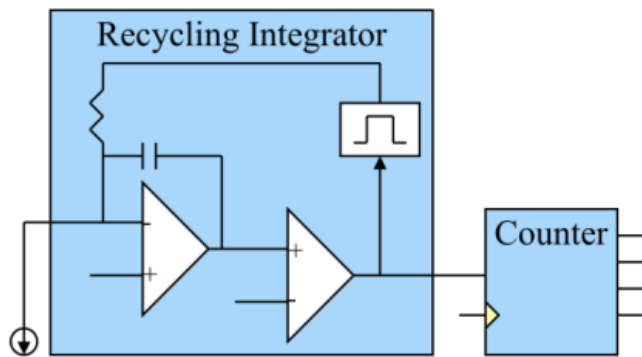
Input current of 150nA



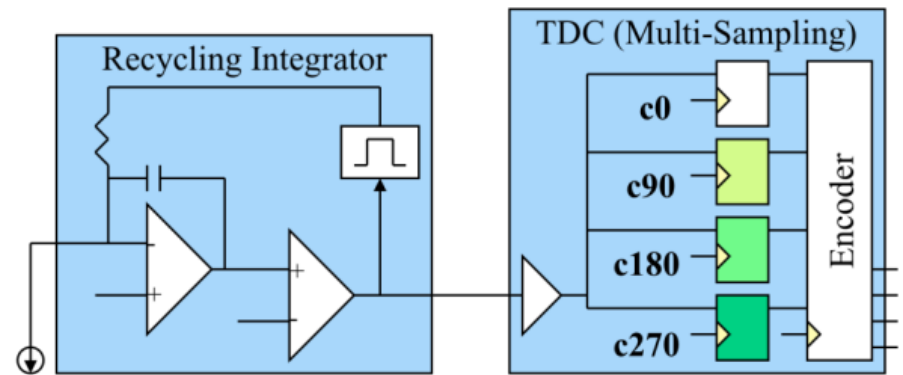
Input current of 300nA

FPGA-based TDC

- Field programmable gate array(FPGA) is a device that can be reconfigured after its fabrication.
- Quartus II as the design software.
- Is needed to measure time between pulses to increase resolution over standard digitalization.
- Time-to-Digital Converter(TDC) gives a time resolution of 1 ns.

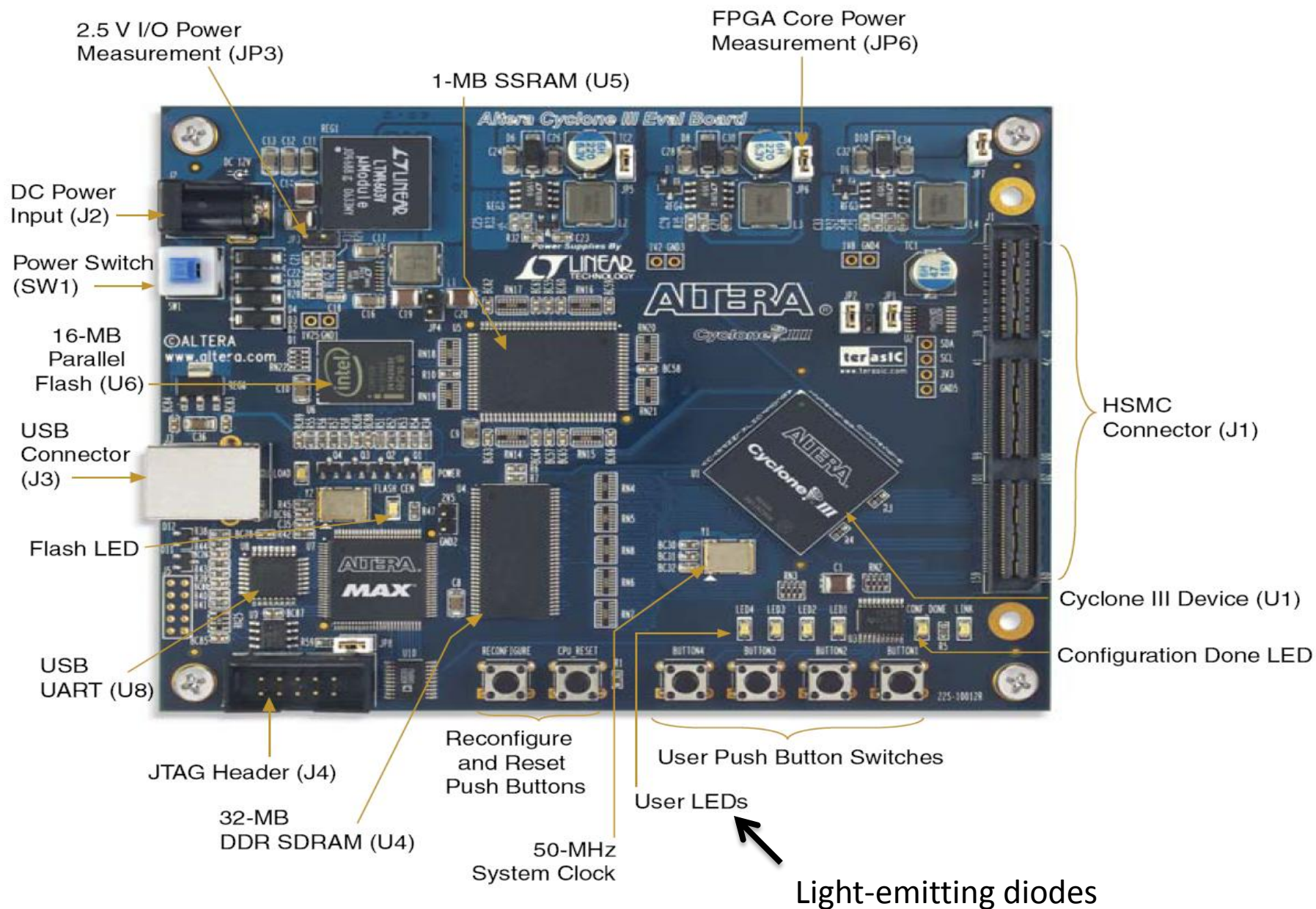


Typical digitalization

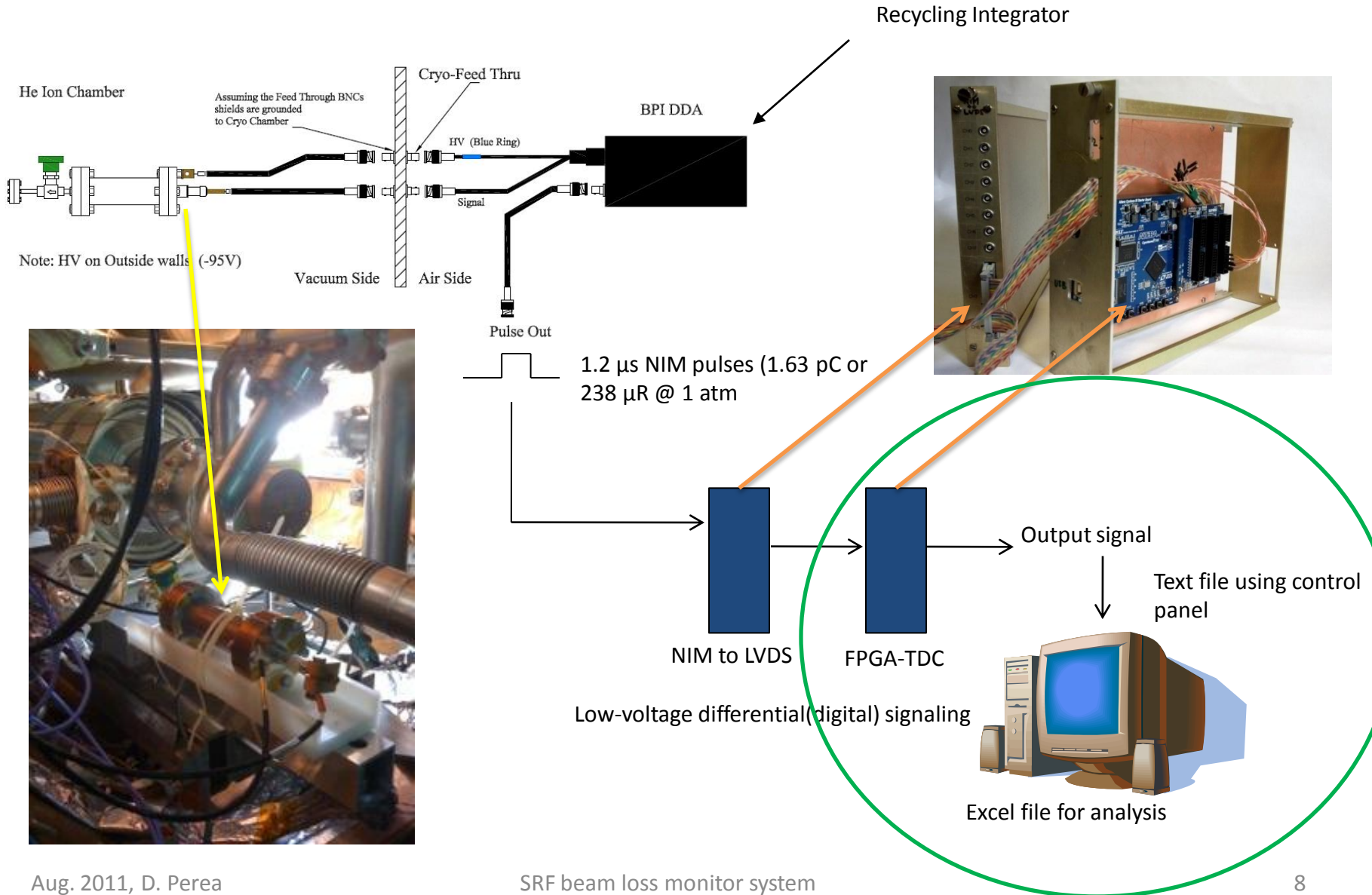


Digitalization with the FPGA

Top View of the Cyclone III FPGA Starter Board



Cryogenic beam loss monitor system display



Objective

Increase the output from a single to multiple (8) channels in the FPGA-based TDC.

- Single channel design
- Schematics (New Blocks)

Quartus Schematic diagram functionality of the extension

Access the SSRAM memory which writes and read the pulses from the chamber.

Button 4 is the switch to start the process

Terasic Control Panel to read out text file

A temporary storage is needed.

Clock inputs

Counters

Counters, clocks as input for each channel

SINGLE CHANNEL

TDC block, 2 storage blocks(leading and falling edge)

2 x

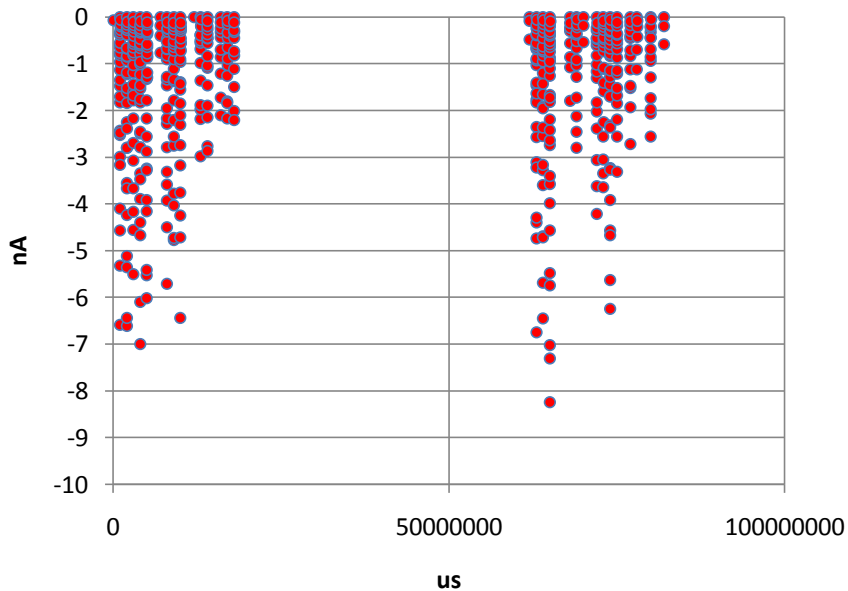
Storage blocks

2 x

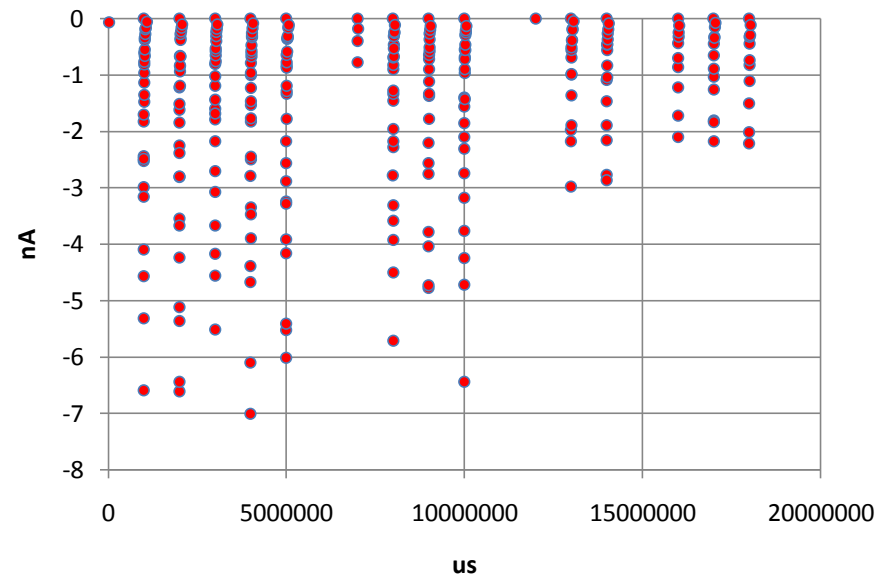
Multiplexer block
=single line

RESULTS

Single Channel



FPGA readout from A0 beam line
when a magnet was swiped
twice.



Closest view of the first swipe of
the magnet. Beam loss was seen
at 1 Hz frequency.

RESULTS

Eight Channels

Microsoft Excel window: NML_BLM3_8Channels.xlsx

Security Warning: Data connections have been disabled

	AF	AG	AH	AI	AJ	AK	AL	AM	AN	AO	AP	AQ	AR	AS	AT	AU	AV	AW	AX	AY
1										CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7	CH 8			
2		65536					0.2887			0.26	0.26	26126.658	3.265E+10	0.257109	0.2573175	0.2573175	1.566E+10			
3																		-1200	-1200	-1
4																				
5	07D4	1956	1956	1959	43490	1955	1953	1954	1953											
6	07D4	55492	55492	55495	55490	55491	55489	55490	55489	12000	12000	12000	0	12000	12000	12000	12000	-195.6	-195.6	-1
7	07D3	43492	43492	43495	1954	43491	43489	43491	43488	12000	12000	12000	0	12000	12000	11999	12000	-5549.2	-5549.2	-55
8	07D3	31492	31491	31495	13954	31491	31489	31491	31488	12000	12000	12000	0	12000	12000	12000	12000	-4349.2	-4349.2	-43
9	07D3	19492	19491	19495	25954	19491	19489	19491	19488	12000	12000	12000	0	12000	12000	12000	12000	-3149.2	-3149.1	-31
10	07D3	7492	7491	7495	37954	7491	7488	7491	7488	12000	12000	12000	0	12000	12000	12000	12000	-1949.2	-1949.1	-19
11	07D3	61078	61077	61031	40054	61077	61076	61077	61074	12000	12000	12000	0	12000	11000	12000	12000	-740.2	-740.1	-7

Digital Pulse Generator

Standard Deviation for the analysis of the distance between pulses has to be between **0 and 0.28**

Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7	Ch 8
0.26	0.26	26126.6582	3.2652E+10	0.25710896	0.25731747	0.25731747	1.5661E+10

CONCLUSION & FUTURE WORK

- From the results we can conclude that the objective is partially achieved due to missing of acceptable standard deviations from three of the eight channels.
- Find the exact problem in channels 3, 4, and 8.
- The final test for the extension will be reading output from the He-Ionization chamber.

Acknowledgments

- Jin-Yuan Wu, Supervisor
- Arden Warner, SRF Dept.
- Elmie Peoples & David Peterson, Mentors
- Dr. James Davenport
- Fermilab, Dianne Engram, Jamieson Olsen & the SIST Committee
- Particle Physics Division (PPD) 14th Floor staff
- Benedict College, Columbia, SC.

Thank you!

Any Questions?

